REMARKS

Claims 1-37 have been examined, with all claims rejected based on prior art.

Claims 36 and 37 have been objected to because of informalities. Applicant believes that the amendment to claim 36 replacing "a first processor core" with "a second processor core" overcomes this objection.

Claims 1-37 have been rejected under 35 USC 102(e) as being anticipated by Subramanian et al. (2002/0015401; hereinafter, "Subramanian I"), and have also been rejected under 35 USC 102(e) as being anticipated by Subramanian et al. (2002/0031166) (hereinafter, "Subramanian II"). Applicant respectfully traverses these rejections for the reasons set forth below.

The present invention is directed to a channel CODEC processor 104 having an algorithm-specific kernel block 212-218, 252-258 operable to receive a data stream, the kernel block comprising logic tailored to perform at least one step of a channel CODEC algorithm on the data stream, and a processor core 210, 250 coupled to provide configuration data to the algorithm-specific kernel block, the configuration data causing the kernel block to perform the at least one step of the channel CODEC algorithm according to one of a plurality of wireless communication standards as specified by the configuration data.

Both Subramanian I and Subramanian II are assigned to the assignee of the present application, Infineon Technologies AG. Neither of these applied references teaches or even suggests the claimed channel CODEC processor. That is, these references do not teach a processor core that provides an algorithm-specific kernel block with configuration data, which causes the kernel block to perform a step of a channel CODEC algorithm according to one of a plurality of wireless communication standards as specified by the configuration data, as required by the claimed invention.

Rather than referring Applicant to specific paragraphs, the Examiner alleges that the claimed invention is taught in 141 paragraphs of Subramanian I (i.e., paragraphs 32-172), and does not refer

to any paragraphs in Subramanian II. While Subramanian I and Subramanian II are each generally concerned with compatibility between protocols, they do not anywhere teach a channel CODEC having processor core providing a kernel block with configuration data, not to mention configuration data which causes the kernel block to perform a step of a channel CODEC algorithm according to one of a plurality of wireless communication standards as specified by the configuration data. Applicant therefore respectfully requests the Examiner to either specifically refer to paragraphs or portions of Subramanian I and Subramanian II where he believes this feature to be taught, or withdraw the prior art rejections.

In view of the above, Applicant believes the pending application is in condition for allowance.

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Respectfully submitted,

By Laura C. Brutman

Laura C. Brutman
Registration No.: 38,395
DARBY & DARBY P.C.
P.O. Box 5257
New York, New York 10150-5257
(206) 262-8919
(212) 527-7701 (Fax)
Attorneys/Agents For Applicant